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IMPLEMENTATION OF LOW POWER EXPLICIT PLUSE- TRIGGERED FLIPFLOP BASED ON SIGNAL FEED THROUGH SCHEME

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ABSTRACT

Power consumption is a key design factor in many circuits. We can say low power concept is a skeleton of electronic industry. The requirement of low power is for consideration of power dissipation and the greatest challenge regarding area and circuit performance. A low power flip-flop design structure is explicit type pulse, trigger and a modified single phase clock is used for signal feed through the scheme. Pulse-triggered FF (PFF) is a single-latch structure that is more advantageous than the conventional transmission gate (TG) and master–slave based FFs in high-speed applications. In this work we have implemented various edges triggered flip-flop and studied their behaviour. We then proposed an Efficient P-FF design solves the long discharging path problem in case of conventional explicit type pulse-triggered FF (P-FF) and achieves better speed and power performance. Based on post-layout simulation results using Micro wind CMOS 90-nm technology, the Efficient P-FF design outperforms the conventional P-FF design in data-to-Q delay. In the meantime, the performance edges on power metrics respectively. Various simulation results based on CMOS 90-nm technology reveals that the Efficient P-FF design is power efficient when the pulse generator is shared with multiple FF's. A better D-to-Q Delay is achieved. Both cadence virtuoso (90 nm technology) and micro-wind version 3.0.0 were used in the study and implementation of the circuits in this work

KEYWORDS: PFF, Flip-Flop, SDFF, HLFF